WHAT IS CLAIMED IS:

1. A method of providing forward error correction (FEC) on a plurality of frame packets, the method comprising:

concatenating selected portions of packet data corresponding to a plurality of frame packets for a first frame;

generating forward error correction bits for the concatenated selected portions of packet data; and

transmitting the forward error correction bits in a separate packet identified with a user data identifier code.

2. The method as defined in Claim 1, wherein the transmission of the forward error correction bits in the separate packet is MPEG-4 compliant.

3. The method as defined in Claim 1, wherein the separate packet is transmitted after the plurality of frame packets.

4. The method as defined in Claim 1, wherein the forward error correction bits are generated using a BCH code.

5. The method as defined in Claim 1, wherein the forward error correction bits are generated using a systematic code.

6. The method as defined in Claim 1, wherein the selected portions of packet data includes motion vector data and DCT data.

7. The method as defined in Claim 1, wherein the selected portions of packet data includes only header data, motion vector data and DCT data.

8. The method as defined in Claim 1, wherein the selected portions of packet data corresponds to packet data located between a resync field and a motion marker.

9. The method as defined in Claim 1, further comprising:

setting a flag indicating that a fixed Video Object Plane (VOP) increment is to be used; and

providing a corresponding fixed time increment value.

10. The method as defined in Claim 1, further comprising transmitting in the separate packet a value for at least a first of the plurality of frame packets related to a quantity of bits within the first packet for which forward error correction bits were generated.

11. An error correction generation circuit, comprising:

a first instruction stored in processor readable memory configured to generate forward error correction data for selected portions of packet data that are to be transmitted in a corresponding plurality of frame packets;

a second instruction stored in processor readable memory configured to store the forward error correction data in a first packet separate from the plurality of frame packets; and

a third instruction stored in processor readable memory configured to identify the first packet with a first data identifier code.

12. The error correction generation circuit as defined in Claim 11, further comprising a fourth instruction configured to concatenate selected portions of packet data before the first instruction generates the forward error correction data.

13. The error correction generation circuit as defined in Claim 11, further comprising a fourth instruction configured to set a flag indicating that a fixed Video Object Plane (VOP) increment is to be used and to provide a corresponding fixed time increment value.

14. The error correction generation circuit as defined in Claim 11, further comprising a fourth instruction configured to provide a Header Extension Code (HEC) in a every packet in a first sequence of packets.

15. The error correction generation circuit as defined in Claim 11, wherein the error correction generation circuit is an integrated circuit.

16. The error correction generation circuit as defined in Claim 11, wherein the first packet is MPEG-4 compliant.

17. The error correction generation circuit as defined in Claim 11, wherein the forward error correction data is generated using a BCH code.

18. The error correction generation circuit as defined in Claim 11, wherein the forward error correction data is generated using a systematic code.

19. The error correction generation circuit as defined in Claim 11, wherein the selected portions of packet data includes motion vector data and DCT data.

20. The error correction generation circuit as defined in Claim 11, wherein the selected portions of packet data includes only header data, motion vector data and DCT data.

21. The error correction generation circuit as defined in Claim 11, wherein the selected portions of packet data corresponds to packet data located between a resync filed and a motion marker.

22. An encoder circuit, comprising:

a means for generating forward error correction data for selected portions of packet data from a plurality of frame packets;

a means for storing the forward error correction data in a first packet separate from the plurality of frame packets; and

a means for identifying the first packet with a first data identifier code.

23. The encoder as defined in Claim 22, further comprising a means for concatenating the selected portions of packet data.

24. The encoder as defined in Claim 22, further comprising a means for transmitting in the first packet at least a first value related to a quantity of bits within the first packet for which forward error correction bits were generated.